National Journal of Multidisciplinary Research and Development
ISSN: 2455-9040
Impact Factor: RJIF 5.22
www.nationaljournals.com
Volume 3; Issue 1; January 2018; Page No. 944-948

Study of body bias on Dopingless SOI

Abhishek Mishra[1], Annu Choudhary[2], Dr. Bhuwan Gupta[3]

[1] Assistant Professor, Department of Electronics and Communication, Modern Institute Technology & Research Centre, Alwar, Rajasthan, India
[2] B.Tech Scholar, Department of Electronics and Communication, Modern Institute Technology & Research Centre, Alwar, Rajasthan, India
[3] Associate Professor, Department of Management Studies, Modern Institute Technology & Research Centre, Alwar, Rajasthan, India

Abstract
In this paper, we study the impact of body bias, gate length, and spacer length on various performance parameters of n-type dopingless Silicon on Insulator transistor (DL-SOI). On-off current ratio (I_{on}/I_{off}) increases with increase in negative body bias voltage. Simulation study shows that subthreshold swing (SS), drain induced barrier lowering (DIBL) are also improved with negative body bias. A comparative study is also performed between junctionless SOI transistor (JL-SOI) and DL-SOI with respect to body bias voltage. Performance parameters such as SS, DIBL, I_{on}/I_{off} are improved in both the devices with negative body bias voltage, but DL-SOI shows higher improvement in I_{on}/I_{off} than JL-SOI with negative body bias voltage. DL-SOI also shows lower threshold voltage variation in comparison to JL-SOI device with body bias voltage.

Keywords: dopingless, drain induced barrier lowering, junctionless, silicon on insulator, subthreshold slope

1. Introduction

Scaling of conventional MOS device puts severe challenges such as short channel effects (SCEs) below 30 nm technology node [1]. Fabrication of p-n junctions with very high doping concentration gradients is another challenging issue below 20 nm technology node. Junctionless transistor addresses above mentioned requirement of formation of ultra sharp junctions in conventional MOSFET. JL-SOI transistor contains uniformly doped source, channel, and drain regions with doping concentration of 10^{-19} cm^{-3} [3]. JL-SOI device gives full CMOS functionally and reduction in short channel effects (SCEs), however, high doping creates the problem of random doping fluctuation (RDF) [4]. Another issue with junctionless device is the requirement of high gate workfunction material to turn-off the device [3, 5].

To address the problems associated with JL-SOI device, dopingless transistor is proposed by [6]. In DL-SOI device, doping concentration is very low almost intrinsic ($N_d=10^{15}$ cm^{-3}) and uniform distributed throughout the device. In DL-SOI device, source and drain regions are fabricated by using charge plasma concept. Charge plasma concept was introduced by [6] for p-n diode. Fabrication of n^+ regions by charge plasma concept does not require any ion implantation [1, 2, 6, 7].

Highly doped devices show higher sensitivity of threshold voltage and SS with respect to the device parameters in comparison to the lightly doped channel [4, 8]. Lightly doped devices show no variation in threshold voltage, SS, and ON current for 10% variation of doping concentration [1]. Both of the devices show equal variation in ON current with respect to the device thickness variations because the characteristics of junctionless device are controlled by depletion region of channel [9].

In this paper, we have reported the comparative study of the effects of body bias on DL-SOI and JL-SOI through 2D TCAD simulations [10]. Sensitivity analysis of performance parameters of DL-SOI with variation of device parameters is also reported in this paper.

2. Device structure and simulations

Fig 1(a)-(b) show the device structure of DL-SOI transistor and JL-SOI transistor. The simulation parameters for DL-SOI transistor are same as JL-SOI transistor except intrinsic silicon body with carrier concentration of $N_d=10^{15}$ cm^{-3}. Threshold voltage is kept constant for both devices. In DL-SOI transistor source and drain regions are induced by using charge plasma concept [1]. In order to induce electron concentration at source and drain regions, the following two conditions must be satisfied:

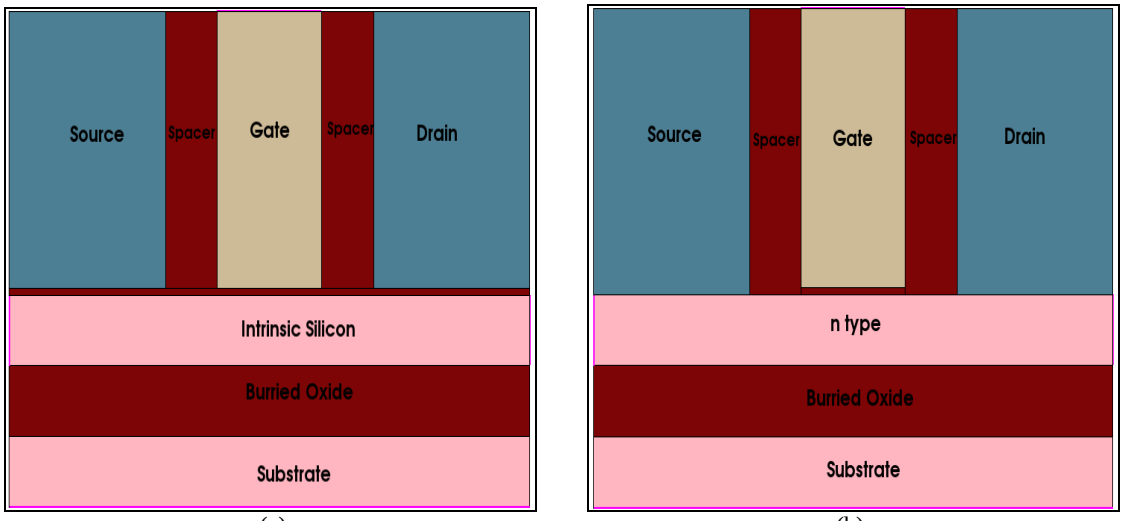
1. Workfunction of source and drain electrode (φ_m) should be less than "$\chi_{Si} + (E_G/2q)$"; where χ_{Si} is the electron affinity of Silicon, E_g is the band-gap of silicon, q is the charge of electron [1].
2. Silicon film thickness should be less than the Debye length $L_D = \sqrt{((\varepsilon V_{th})/qN)}$, where V_{th} is threshold voltage, ε is the dielectric constant of silicon [1].

In DL-SOI device, metal with workfunction of 3.9 eV is used as source and drain electrode to induce n^+ regions [1]. The other parameters of both devices are given in the table below.

Lombardi mobility model along with Shockley- Read-Hall (SRH) and Auger recombination model is used for simulations. Lombardi's mobility model shows the effect of mobility degradation due to surface acoustic phonon and surface roughness scattering. SRH model introduced the effect of defects on recombination of electrons, holes and trapped carriers [10].

Table 1: Device parameters for simulation

Parameters	JL-SOI	DL-SOI
Silicon thickness	10 nm	10 nm
Effective oxide thickness (EOT)	1 nm	1 nm
Gate workfunction	4.7 ev	5.5 ev
S/D Extension	10 nm	10 nm
Gate length	20 nm	20 nm
Buried Oxide thickness (t_{box})	10 nm	10 nm



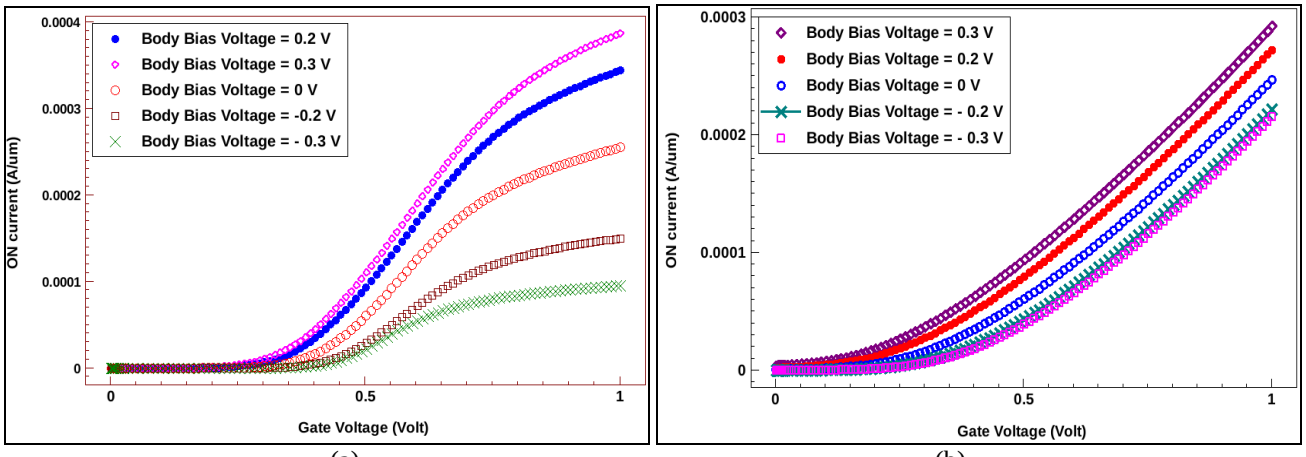
(a) (b)

Fig 1: (a) DL SOI Structure (b) JL SOI Structure

3. Body bias variation

Fig. 2 and Fig.3 show the effects of body bias on both of the devices. On current decreases with negative body bias voltage in both of the devices as shown in Fig.2 (a)-(b). Negative body bias voltage accumulates negative charge density in depletion region under gate which increases the threshold voltage [8]. Fig.3 (a) shows the variation of threshold voltage with respect to body bias voltage. Negative body bias voltage increases the control of gate over channel that increases the I_{on}/I_{off} ratio and improves SS, DIBL as shown in Fig. 3 (b)-(d).

JL-SOI shows higher variation in threshold voltage than DL-SOI. DL-SOI shows higher improvement in SS, DIBL, I_{on}/I_{off} with negative body bias voltage than JL-SOI.



(a) (b)

Fig 2: Transfer characteristics of (a) DL-SOI (b) JL-SOI with respect to body bias voltage

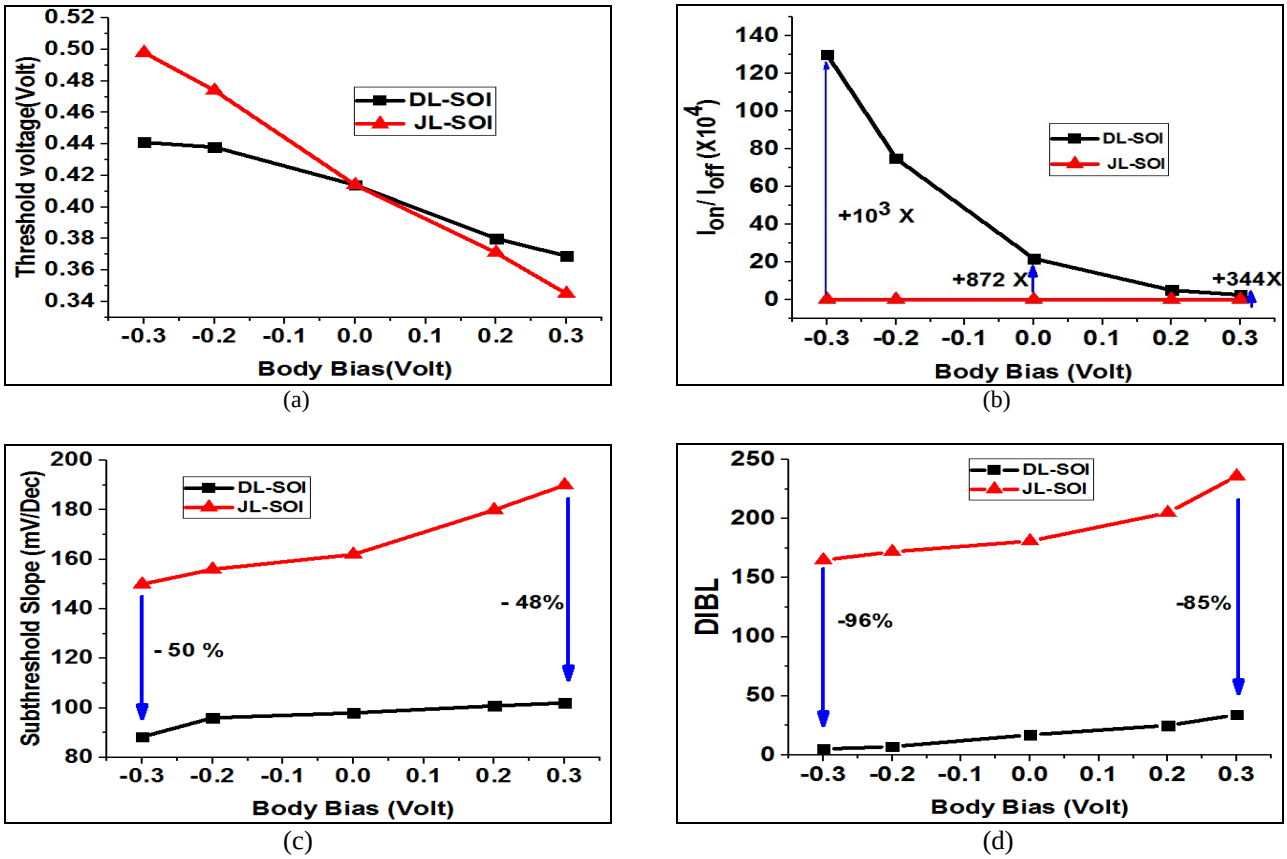


Fig 3: Variation of (a) V_{th} (b) I_{on}/I_{off} (c) Subthreshold Slope (d) DIBL with respect to body bias voltage.

4. Gate length variation

Fig.4 (a)-(d) shows the variation of V_{th}, SS, I_{on}/I_{off} ratio and DIBL. As the gate length increases SS, I_{on} and I_{off} decrease, while I_{on}/I_{off} and V_{th} increase. The lateral electric field influences the electrostatic of the channel due to which threshold voltage reduces. This reduction in V_{th} is known as V_{th} roll-off.

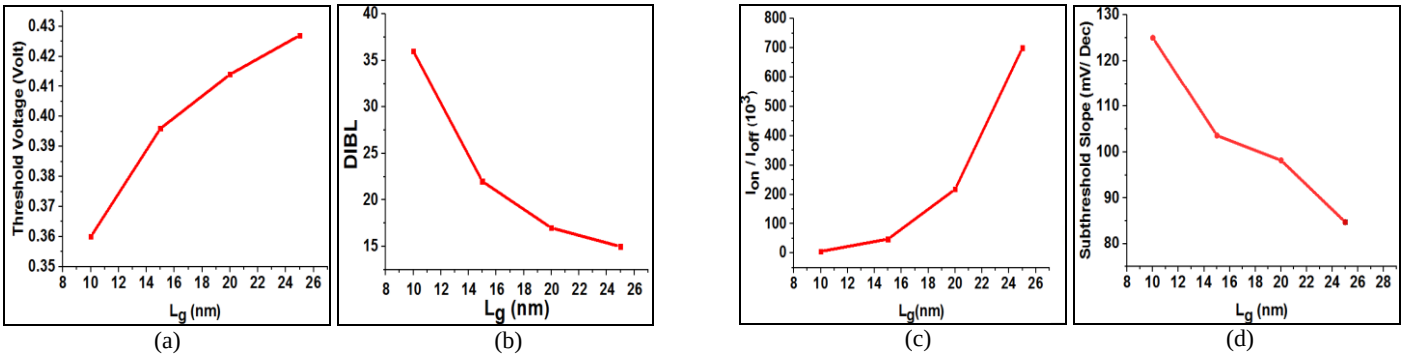
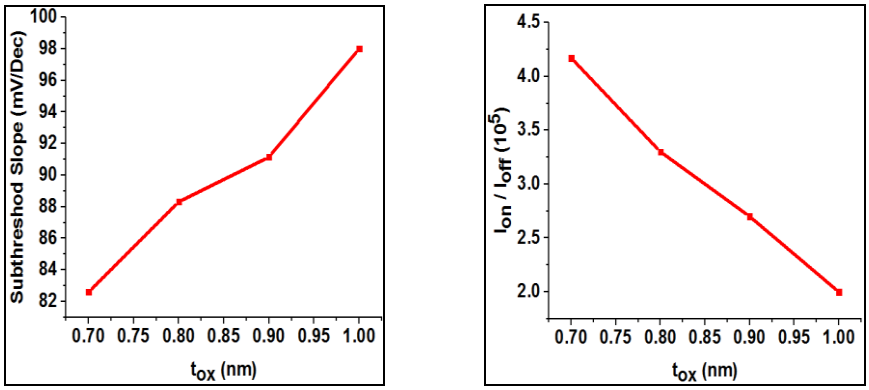


Fig 4: Variation of (a) Threshold voltage (b) DIBL (c) I_{on}/I_{off} (d) Subthreshold Slope with gate length of DL-SOI.

5. Gate oxide thickness variation

V_{th} variation is negligible with change in gate oxide thickness, but on current increases with decreasing oxide thickness. Variation in subthreshold swing and I_{on}/I_{off} ratio of is shown in the Fig. 5 (a)-(b).

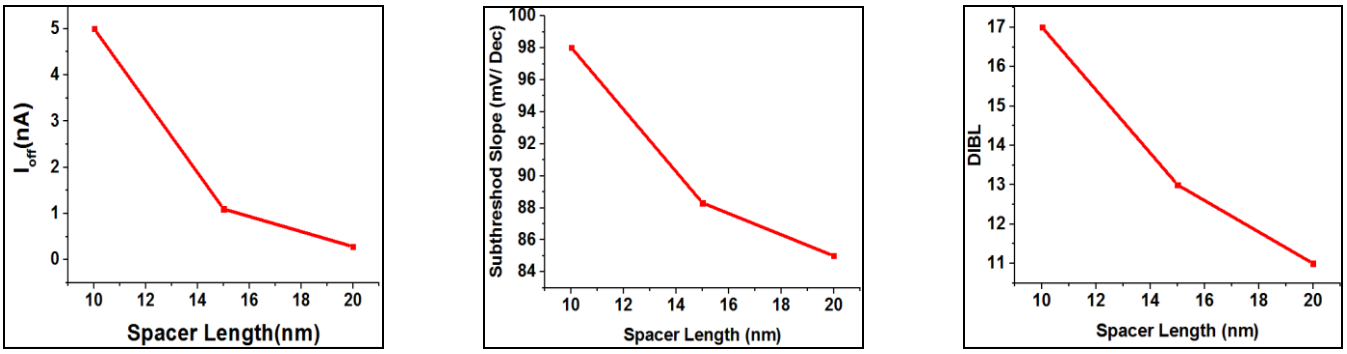


(a) (b)

Fig 5: Variation of (a) Subthreshold Slope (b) I_{on}/I_{off} with respect to oxide thickness of DL-SOI.

6. Spacer length variation

Larger spacer length increases the effective gate length, which increases the control of gate over channel and reduces the I_{off}. SS and DIBL are improved with increasing spacer length. Effect of variation of spacer length on performance parameters is shown in Fig.6 (a)-(c).



(a) (b) (c)

Fig 6: Variation of (a) I_{off} (c) Subthreshold Slope (c) DIBL with respect to spacer length of DL-SOI

7. Conclusion

Effects of negative body bias voltage on DL-SOI and JL-SOI devices are reported in this paper. It is concluded that JL-SOI shows higher variation in threshold voltage with body bias than DL-SOI. DL-SOI and JL-SOI device show variation of threshold voltage by 6% and 20% respectively at body bias of -0.3V. Both of the devices shows reduction in I_{off} and increase in I_{on}/I_{off} ratio with negative body bias voltage. However, DL-SOI shows higher improvement in (I_{on}/I_{off}) ratio than JL-SOI. I_{on}/I_{off} ratio is 10^3 times higher in DL-SOI in comparison to JL-SOI device at body bias of -0.3V. Other performance parameters such as DIBL, SS are also improved with negative body bias voltage, but DL-SOI shows higher improvement in performance parameters in comparison to JL-SOI. DL-SOI and JL-SOI devices show reduction in DIBL by 71% and 12% at body bias of -0.3V, respectively.

8. References

1. Sahu C, Singh J. Charge-plasma based process variation immune junctionless transistor, IEEE Electron Device Lett., 2014; 35(3):411-413.
2. Sahu C, Ganguly A, Singh J. Design and performance projection of symmetric bipolar charge-plasma transistor on SOI, Electron. Lett, 2014; 50(20):1461-1463.
3. Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, *et al*. Nanowire transistors without junctions, Nat. Nanotechnol. 2010; 5(3):225-229.
4. Rao R, Das Gupta N, Das Gupta A. Study of random dopant fluctuation effects in FD-SOI MOSFET using analytical threshold voltage model, IEEE Trans. Device Mater. Rel. 2010; 10(2):247-253.
5. Colinge JP, Kranti A, Yan R, Lee CW, Ferain I, Yu R, *et al*. Junctionless Nanowire Transistor (JNT): Properties and design guidelines, Solid-State Electronics, 2011; 65-66; 33-37.
6. Sahu C, Singh J. Device and circuit performance analysis of double gate junctionless transistors at Lg = 18 nm. IET J Eng. 2014; 1:1-6.
7. Hueting RJE, Rajasekharan B, Salm C, Schmitz J. The charge plasma P-N diode, IEEE Electron Device Lett., 2008; 29(12):1367-1369.
8. Sung_Mo Kang, Yusuf Leblebici. MOS Transistor, in CMOS Digital Integrated Circuits, 3th ed. New York: McGraw-Hill, 2003, pp. 76-80.
9. Jagadesh Kumar M, Kanika Nadda. Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device IEEE Trans. On Electronic Devices, 2012; 59(4).
10. Sentaurus TCAD User Manual, 2014. Synopsys, Inc. [Online]. Available: www.synopsys.com
11. Boucart K, Ionescu AM. Length scaling of the double

gate tunnel FET with a high-K gate dielectric, Solid-State Electron., 2007; 51(11-12):1500-1507.
12. Jagadesh Kumar M, Sindhu Janardhanan. Doping-less Tunnel Field Effect Transistor: Design and Investigation IEEE Trans. On Electronic Devices, 2013; 60(10):3285-3290.
13. Bijoy Rajasekharan Raymond JE Hueting, Cora Salm, Tom van Hemert, Rob A. M. Wolters, and Jurriaan Schmitz, Fabrication and Characterization of the Charge-Plasma Diode IEEE Trans. On Electronic Devices, 2010; 31(6).
14. Ishu Agrawal, Kondekar PN. Drain Current improvement using spacer, charge plasma concept IEEE ISCE 2014 1569954437.
15. Loan SA, Bashir F, Rafat M, Alamoud AR, Abbasi SA. A high performance charge plasma PN-Schottky collector transistor on silicon-on-insulator, Semicond. Sci. Technol., 2014; 29(9):095001.
16. Bashir F, Loan SA, Rafat M, Alamoud AR, Abbasi SA. A high performance no. gate engineered charge plasma based tunnel field effect transistor. J Comput. Electron. 2015; 14(2):477-485.
17. Loan SA, Bashir F, Rafat M, Alamoud AR, Abbasi SA. A high performance charge plasma based lateral bipolar transistor on selective buried oxide, Semicond. Sci. Technol., 2014; 29(1):015011.
18. Singh S, Kondekar PN. Dopingless super-steep impact ionization MOS (dopingless-IMOS) based on workfunction engineering, Electronics Letters 5th June 2014; 50(12):888-889.
19. Zhuojun Chen, Yongguang Xiao, Minghua Tang, Ying Xiong, Jianqiang Huang, Jiancheng Li, *et al*. Surface-Potential-Based Drain Current Model for Long-Channel Junctionless Double-Gate MOSFETs, IEEE Traansactions on electronics Devices, 2012; 59(12).
20. Yi-Bo Liao, Meng-Hsueh Chiang, Yu-Sheng Lai, Wei-Chou Hsu. Stack Gate Technique for Dopingless Bulk FinFETs, IEEE Traansactions on electronics Devices, 2014; 61(4).